ALLEVIATING TIMING BASED CONGESTION WITHIN CIRCUIT DESIGNS

ABSTRACT

A method of relieving timing-based congestion during physical implementation of a programmable logic device can include routing a placed circuit design for the programmable logic device in a delay mode and calculating an initial delay for connections of the circuit design based upon said routing step. A final delay for connections of the circuit design can be predicted were connection overlaps to be removed. Connections of the circuit design that do not conform with timing constraints based upon at least one of the initial and final delays can be identified. Accordingly, a detailed routing of the circuit design or further optimization of the circuit design can be selectively performed according to the determination regarding the timing constraints.